REMARKS/ARGUMENTS

Reconsideration is respectfully requested.

The Abstract of the Disclosure has been revised to a single paragraph with about 150 words. Objection to the Abstract is respectfully requested.

Claims 1-5 are pending in the present application before this amendment. By the present amendment, Claim 1 has been amended, and Claim 6 has been added. No new matter has been added.

Claims 1-5 stand rejected under 35 U.S.C. § 112, ¶2 as being indefinite. It is noted that both interpretations in the Office Action, page 2, are congruous to the operations of the present invention. Nevertheless, Claim 1 has been amended for further clarification (see the Specification page 8, lines 12-15 and FIG. 6). Withdrawal of the rejection is respectfully requested.

Claims 1-2 and 4-5 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,373,766 (Birk). The "et al." suffix, which may appear after a reference name, is omitted in this paper.

Applicants respectfully point out that the Office Action on page 3 rather inaccurately characterizes the teachings of Birk. Birk relates to providing an improved type of sense amplifier (the elements 120 in FIGS. 2-3) that is capable of detecting more than just two voltage levels, i.e., high or low (see Birk col. 5, lines 1-45). To accomplish this task, Birk teaches its own modified version of sense amplifier 120' (FIG. 3), which can be contrasted with a conventional sense

amplifier such as the element 120 in FIGS. 1A and 3 of Birk.

General operations of a sense amplifier in a conventional DRAM can be described with respect to FIGS. 1A and 3 of Birk, because FIGS. 1A and 3 of Birk may be understood as showing a generalized, conventional basic DRAM core operation utilizing the conventional sense amplifiers (except 120' in FIG. 3).

Generally, the bit lines in a DRAM are ordinarily precharged in anticipation of a sensing operation by a sense amplifier, and in the same manner, Birk's bit lines (FIG. 3, elements BL, BL*, BR, BR*) are precharged by VBLP, which is usually $V_{DD}/2$. The CS (FIG. 3 of Birk) is the storage capacitor of a DRAM memory cell that holds the charges to signify the bit data. When a word line (WLRj or WLR(j+1) in FIG. 3 of Birk) is activated, depending on the charge status of CS, the sense amplifier would sense high or low in the case of a conventional sense amplifier (e.g, greater than $V_{DD}/2$ or less than $V_{DD}/2$) or one of multi-level references in the case of Birk.

Thus, the assertions made in the Office Action page 3 are incorrect. In particular, Birk's 120 is not comparable to the claimed voltage output means, because Birk's 120 is simply a conventional sense amplifier, which is also well illustrated in FIG. 1A of Birk. The assertion that VBLP is comparable to the claimed voltage for driving the sense amplifier is incorrect, since use of VBLP in Birk's is no different than a conventional one, i.e., for precharging the bit line. The combination of TS and CS and VCP in Birk does not comprise the claimed first core

voltage step up means, since the combination merely represents a typical charge storage cell in a memory.

The presently claimed invention (i.e., FIG. 6, element 600 showing an embodiment) is **not at all** what is taught by Birk. Birk's teachings may arguably relate to the conventional core area 120 as shown in FIG. 1, the prior art example, of the present application, but Birk fails to anticipate the presently claimed invention that relates to an embodiment as shown in FIG. 6, element 600.

According to the presently claimed invention, the precharge voltage VBLP is half the core voltage VCORE. As shown in FIG. 7 of the present application, the sense amplifier senses the changes in the VBLP in presence of, inter alia, the word enable and sense amplifier enable signals.

The presently claimed invention includes the first and second core voltage step-up means (such as FIG. 6, 602 and 603) connected between a power supply (such as VDD) and the node (such as N1) that solves the problems associated with the conventional system of FIG. 2 by, for example, providing the two-step, step-up voltages. This provides faster operations but also better power consumption characteristics and reduced power noise when compared to the conventional systems.

For the reasons above, Birk fails to teach (or remotely suggest) even one claimed element recited in Claim 1.

Applicants generally agree with the Office Action with respect to the

allowable Claim 3 that the "prior art of record fails to teach or fairly suggest a first core voltage step-up means[, which] comprises a transistor that is smaller than the transistor of the second core voltage step-up means." However, numerous other grounds of allowabilty are also present in view of Birk's teachings since Birk does not relate to the claimed structure of the voltage drivers of the present application (such as 601, 602, 603 in FIG. 6).

For the reasons set forth above, Applicants respectfully submit that Claims 1-6, now pending in this application, are in condition for allowance over the cited reference. This amendment is considered to be responsive to all points raised in the Office Action. Accordingly, Applicants respectfully request reconsideration and withdrawal of the outstanding rejections and earnestly solicit an indication of allowable subject matter. Should the Examiner have any remaining questions or concerns, the Examiner is encouraged to contact the undersigned attorney by telephone to expeditiously resolve such concerns.

Respectfully submitted,

Dated: September 13, 2004

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